 

**Shock Testing Flip-Chip Interconnects:** Increasingly sophisticated electronic systems are being more widely deployed in harsh, real-world applications such as automotive, avionics, industrial production and others. That means thermal/mechanical issues like heat, vibration and shock are more critical because of their potential reliability impacts. But existing shock/vibration test methods and equipment are falling short because they were designed for less complex electronic systems. At ECTC, TU Dresden researchers will describe better ways to simulate and perform shock testing under real-world conditions. They will unveil a new test vehicle for shock and other mechanical loads, which can test multiple components simultaneously. In the initial design, their test board consisted of nine flip-chips (2.9 x 4.9mm²) mounted in a 3x3 matrix configuration. They were tested until failure under shock loads of 130g amplitude/2ms pulse width, and at -40°C, room temperature, and 125°C. Failure analysis after the tests showed crack initiation, propagation and even some complete cracks near the solder joints on both the flip-chip and board sides of the joints. The researchers say these results will serve as a basis for better shock profiles, measurement practices and fixture methods for future testing, and for testing with a mixture of loads as well.

**The images above show**:

* At left (a) is the newly developed test board; (b) is the flip-chip array; and (c) is the flip-chip test component.
* At right are cross-sectional photos of the various damage states seen in the solder joints.

**(Paper 18.7, “*Isothermal Shock Testing on Flip-Chip Interconnects*,” M. Häusler et al, TU Dresden)**